PRESS RELEASE

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CHIP MANUFACTURING PROCESS IS ON A VERGE OF A BREAKTHROUGH

PROMISING APPROACH TO MANUFACTURE A NEW GENERATION OF COPPER INTERCONNECTS

An international and interdisciplinary team searches for a way of non-aqueous direct-on-barrier copper plating, which will support further device scaling in sub-32 nm technologies.

Moore's Law marches on – recognisable by the increasing circuit density, hybrid chips and progressive scaling. However the semiconductor industry has arrived at a point where the scaling laws become more and more scientific challenges. Specific issues are the increasing process variability, the expected physical and reliability limitations of devices and in interconnects as well as the need for new characterisation methods and techniques.

The CopPeR project is a collaborative project, which is co-financed by the European Commission under the 7th Framework Programme. It started in January 2008 and is running for 30 months. The acronym 'CopPeR' stands for 'Copper Interconnects for Advanced Performance and Reliability". The project aims to develop a novel copper deposition process based on the use of non-aqueous solvents in order to overcome the limitations of currently applied interconnect formation processes enabling device scaling beyond the 32 nm technology node. This non-aqueous process will open novel routes to implement direct-on-barrier plating, focussing on tantalum and ruthenium as diffusion barriers. The process developed and implemented within the CopPeR project will significantly improve the quality of the Cu metallization due to the fact that the conductivity limiting seed-Cu will be eliminated and thinner barrier films can be applied, e.g. by ALD (atomic layer deposition); so more volume is available in trenches for high quality, low resistivity Cu.

The project consists of three phases: In the first phase, electrolyte ingredients and wafer materials will be selected, basic physical properties investigated and a deposition cell designed through modelling and simulation as well as new analytical techniques evaluated to enable adequate analysis of the deposited films. The second phase will focus on the development of the copper deposition process based on the findings from phase one with the additional support of micro-modelling and the process scaled and integrated into a 300 mm proof-of-concept. In the third and final phase, the process will be integrated into a complete interconnect scheme, and optimized according to the industrial chip manufacturer's needs.

The final goal of the CopPeR project will be achieved through collaborations within a very strong consortium based on a team with outstanding scientific, engineering and manufacturing qualifications. The consortium consists of 8 European leading companies and academic institutions in the area of plating technologies (Technikon Forschungs- und Planungsgesellschaft mbH (AT), SEZ AG (AT), Katholieke Universiteit Leuven (BE), Technische Universität Graz (AT), ELSYCA N.V. (BE), Vrije Universiteit Brussel (BE), Infineon Technologies AG (G) and Cormet OY (FIN)). Together they represent a vertically integrated consortium, with knowledge stretching from basic research to the design and marketing of products. This includes the production, evaluation and impacts on the ITRS Roadmap of all parts targeted by the project as well as intimate knowledge of the end-user market.

For more information about the CopPeR project please visit the project's website ***http://www.copper-project.eu*** *or send an e-mail to* ***coordination@copper-project.eu***

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