

The main objective of the project is the implementation of a unique copper deposition process, which will allow further scaling of interconnects.

The CopPeR-Project:

The CopPeR project will provide a novel copper deposition process based on the use of non-aqueous solvents to overcome the limitations of currently applied interconnect formation processes enabling device scaling beyond the 32 nm technology node.

The project aims to develop a novel copper deposition process based on the use of non-aqueous solvents in order to overcome the limitations of currently applied interconnect formation processes enabling device scaling beyond the 32 nm technology node. This non-aqueous process will open novel routes to implement direct-on-barrier plating, focussing on tantalum and ruthenium as diffusion barriers. The process developed and implemented within the CopPeR project will significantly improve the quality of the Cu metallization due to the fact that the conductivity limiting seed-Cu will be eliminated and thinner barrier films can be applied, e.g. by ALD (atomic layer deposition); so more volume is available in trenches for high quality, low resistivity Cu.

Motivation:

The semiconductor industry has arrived at a point where the scaling laws are starting to drive more scientific than engineering challenges. Specific issues are the increasing process variability, the expected physical and reliability limitations of devices and in interconnects as well as the need for new characterisation methods and techniques.

Long term challenges to enhance interconnect performance at and beyond the 32 nm node deal with substantially sophisticated tasks:

- › introducing novel interconnect schemes
- › introduction of new interconnect processes and materials
- › enhanced modelling and simulation techniques for several applications

Overall Strategy:

Phase 1 - Materials and Design

- › Definition of Requirements and specifications
- › Selection of electrolyte and wafer materials
- › Investigation of basic physical properties
- › Design of the first 300mm cell

Phase 2 – Process Development

- › Development of the seedless copper deposition
- › macro- and micro-model simulations and nano-characterisation methods
- › Manufacturing of a 300mm prototype

Phase 3 – Implementation and testing

- › Implementation of the copper deposition process into a complete interconnect scheme
- › mechanically and electrically testing on fully integrated test structures

Objectives:

The CopPeR project targets the mid- and long-term challenges of introducing new interconnect materials and deposition techniques for the 32 nm, 22 nm and 18 nm technology nodes.

The main objective of the project is to overcome these challenges by the implementation of a unique copper deposition process, which will allow further scaling of interconnects. The research will be complemented with evaluation of the results on production scale demonstrators.

Technical Approach:

The work plan of CopPeR includes six work packages:

- WP1:** Material Requirements and Specification
- WP2:** Simulation Based System Quantification and Scale-Up
- WP3:** Copper Deposition from Non-Aqueous Solvents
- WP4:** Proof-of-Concept
- WP5:** Instrumentation and Metrology for Nano-characterisation
- WP6:** Project Management, Dissemination and Standardisation





Contact:

Project Coordinator

Klaus-Michael Koch
 Technikon Forschungs- und Planungsgesellschaft mbH
 Burgplatz 3a
 9500 Villach
 Austria
 Tel.: +43 4242 23355 - 0
 Fax: +43 4242 23355 - 77
 E-Mail: coordination@copper-project.eu
 Web: www.copper-project.eu

Technical Project Leader

Harald Okorn-Schmidt (LAM Research AG)

Project Management Leader

Ulrike Schnitzer (Technikon)

www.designation.at

CopPeR Copper Interconnects for Advanced Performance and Reliability

The Consortium:

CopPeR will achieve the final goal through collaborations within a very strong consortium based on a team with outstanding scientific, engineering and manufacturing qualifications. The Copper consortium brings together Europe's leading companies and academic institutions in the area of semiconductor technologies and material sciences. The representatives of each partner are experienced researchers with positions authorising them to manage the resources needed for the project.



The consortium is constituted of 8 partners from 4 European countries:

1



LAM Research AG
 (Austria)

2



Katholieke Universiteit Leuven -
 MTM-KUL (Belgium)

3



FELMI - Technische Universität
 Graz (Austria)

4



ELSYCA N.V.
 (Belgium)

5



Vrije Universiteit Brussel -
 Department ETEC (Belgium)

6



Technikon Forschungs- und Pla-
 nungsgesellschaft mbH (Austria)

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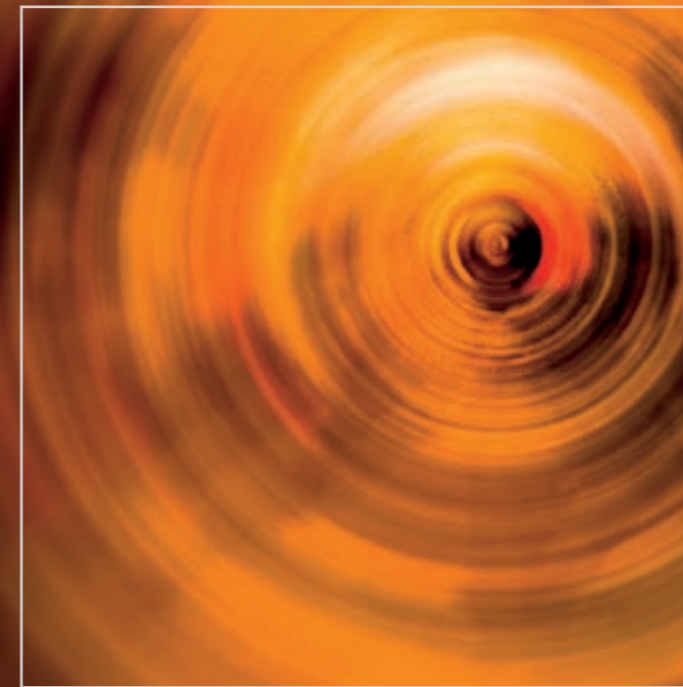


Infineon Technologies AG
 (Germany)

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Cormet OY
 (Finland)



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